SRS test diagram draft figure for MMF ad hoc, post review

27 March 2014 jpk

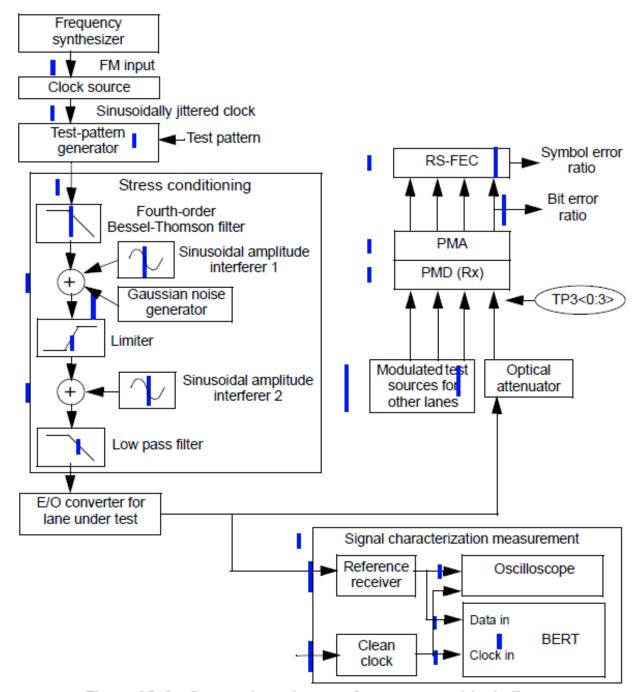


Figure 95-3—Stressed receiver conformance test block diagram

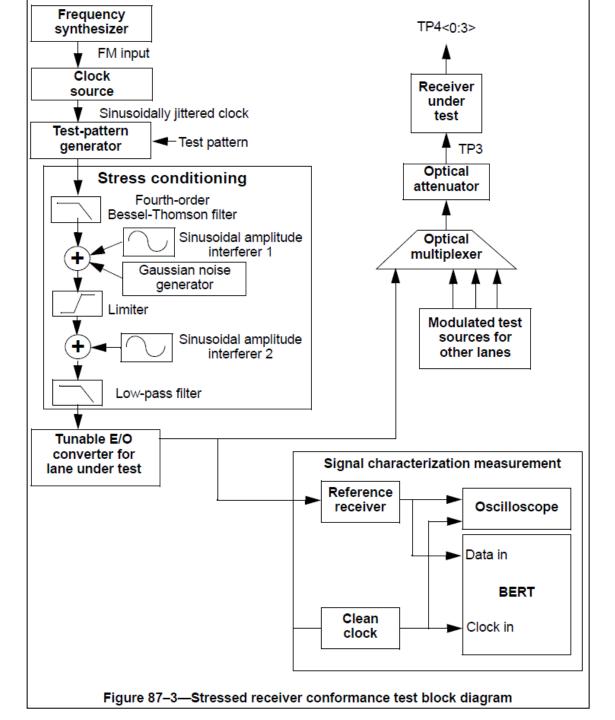
95.8.8 text should say

- Can either measure error ratio at the PMD/PMA interface
- Or measure errored symbols at the input to the RS-FEC

Slides shown during review

Frequency System under synthesizer test FM input Clock PCS or WIS Test pattern (Rx) source Sinusoidally jittered clock PMA (Rx) Test-pattern Optical generator PMD (Rx) TP3 attenuator Stress conditioning E/O Signal characterization converter measurement Stress conditioning Fourth-order Bessel-Thomson filter Signal characterization measurement Sinusoidal amplitude interferer Oscilloscope Clean clock Clock in Reference Data in Rx

Figure 52-10—Stressed receiver conformance test block diagram



Frequency synthesizer Symbol error FM input ratio Clock source Sinusoidally jittered clock **RS-FEC** Test-pattem 🖥 bit error Test pattern generator **PMA** ratio PMD (Rx) Stress conditioning TP3<0:3> Fourth-order Bessel-Thomson filter Sinusoidal amplitude interferer 1 Gaussian noise generator Limiter Opt Sinusoidal amplitude atten interferer 2 Low pass filter Modulated test sources for other lanes E/O convertor for lane under test Signal characterization measurement Reference oscilloscope receiver Data in BERT Clean Clock in clock Figure 95-3—Stressed receiver conformance test block diagram